

PREPARED BY: _____ DATE _____	<h1>SHARP</h1> <p>ELECTRONIC COMPONENTS GROUP SHARP CORPORATION</p> <h2>SPECIFICATION</h2>	SPEC No. LC63709
APPROVED BY: _____ DATE _____		FILE No. _____
		ISSUE Jul. 11, 1988
		PAGE 14 Pages
		REPRESENTATIVE DIVISION <input type="checkbox"/> IC DIV. <input type="checkbox"/> SEMICONDUCTOR APPLICATION DIV. <input checked="" type="checkbox"/> LCD DIV. <input type="checkbox"/> ELECTRONIC COMPONENTS DIV. <input type="checkbox"/>

DEVICE SPECIFICATION FOR

Dot Matrix LCD Unit  
(20-character/2-line Display  
STHC gray type)

MODEL No.

LM20A21

CUSTOMER'S APPROVAL

DATE \_\_\_\_\_

BY \_\_\_\_\_

PRESENTED

BY H. Nakajima

H. Nakajima<sup>✓</sup>  
 Department General Manager  
 Engineering Department  
 LCD Division  
 ELECOM Group  
 SHARP CORPORATION

**SHARP**LM20A211. Overview

The **LM20A21**, dot-matrix LCD unit consists of a 5 x 7-dot 20-character 2-line dot-matrix LCD panel, LCD driver and controller LSI fabricated on a single PCB. Incorporating mask **ROM-based** character generator and display data **RAM** in the controller LSI, the unit can efficiently display the desired characters under microprocessor control.

(Features)

- (1) The LCD of the unit is **STHC (Super Twisted High Contrast)** gray type.
  - (2) Low power consumption with the dot-matrix LCD panel and CMOS LSI.
  - (3) Thin, lightweight design permits easy installation in a **variety** of equipment.
  - (4) Allowing for being connected at general-purpose CMOS signal level, the unit can be easily interfaced to a microprocessor with common 4-bit and 8-bit parallel inputs and outputs.
  - (5) Built-in character generator **ROM** and RAM, and display data RAM:
    - Character **generator ROM**  
160 different 5 x 7 dot-matrix character patterns  
(Alphanumeric and symbols)
    - Character generator **RAM**  
8 different user programmed 5 x 7 dot-matrix patterns
    - Display data **RAM**  
80 x 8 bits
  - (6) Numerous instructions  
Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Blink character, Cursor shift, Display shift
  - (7) Built-in reset circuit is triggered at power ON.  
(For the operating conditions, refer to the separate user's manual "Dot-Matrix LCD Units with built-in controllers".)
  - (8) The unit operates from a single 5V power supply.
- \* As to the **packing**, refer to the separate "COMMON PACKING SPECIFICATION FOR LM20255 series".

**SHARP****2. Construction and Outline**

Construction : 5 x 7 dots + cursor, 20-character 2-line dot-matrix display unit

Outline : See Fig. 7.

Interface signals : See Table 5.

Character pattern details : See Fig. 7.

Character codes : See Table 8.

There shall be no scratches, stains, chips, distortions and other external **drawbacks** that may affect the display function.

Rejection criteria shall be noted in Inspection Standard ( s-u- 009 ).

**3. Mechanical Specifications**Table 1

Parameter	Specification	Unit
Outline dimensions	115 (W) X 36(H) X11 MAX(D)	mm
Effective display area	83(W) X 18.6(H)	mm
Display format	20 characters X 2 lines	
<b>Character</b> format	5 X 7 dots with cursor	
Character size	3.2(W) X 4.85 (H) (5 X 7 dots)	mm
Dot size	0.6(W) X 0.65(H)	mm
Dot spacing	0.05	mm
Character color *	Dark blue	
Background color*	Gray	
Weight	Approx. 40	g

\* Due to the characteristics of the LC Material, the colors vary with environmental temperature.

**SHARP**4. Electrical Specifications

## 4.1 Absolute maximum ratings

Table 2

Parameter	Symbol	Hin.	Max.	Unit	Remark
Supply voltage(Logic)	$V_{DD} - V_{SS}$	-0.3	+6.5	V	
Supply voltage (LCD drive)	$V_O - V_{SS}$	0	+6.5	v	$V_{DD} > V_O$
Input voltage	$V_{IN}$	-0.3	$V_{DD} + 0.3$	V	
Storage temperature	Tstg	-25	+70	“C	
Operating temperature	Topr	0	+50	“C	

## 4.2 Electrical characteristics

Table 3

(Ta = 25°C)

Parameter	Symbol	Min.	Typ.	flax.	Unit	Condition	
Supply voltage (Logic)	$V_{DD} - V_{SS}$	4.75	5.0	5.25	v		
Supply voltage (LCD drive)	$V_O - V_{SS}$		0.5		v	$V_{DD} = 5.0V$	
Input voltage	" L "	$V_{IL}$	-0.3	-	0.6	v	
	" H "	$V_{IH}$	2.2	-	$V_{DD}$	v	
Output voltage	" L "	$V_{OL}$			0.4	v	$I_{OL} = 1.2mA$
	" H "	$V_{OH}$	2.4	-	-	v	$-I_{OH} = 0.205mA$
Input leakage current	$I_{IL}$			1	$\mu A$		
Internal oscillating frequency	fosc		250		KHz		
Supply current	$I_{DD}$		1.8	2.5	mA	$V_{DD} = 5V$	
Power dissipation	Pd		9	12.5	mW	$V_O = 0V$	

**SHARP**

4.3 Timing characteristics

Table 4

$V_{DD}=5.0V \pm 5\%$

$T_a = 0 \sim 50^\circ C$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Enable cycle time	$t_{cycE}$	1000	-	-	ns
Enable pulse width	$PW_{EH}$	450	-	-	ns
Enable rise/fall time	$t_{Er}, t_{Ef}$	-		25	ns
RS, R/W setup time	$t_{AS}$	140	-	-	ns
Address hold time	$t_{AH}$	10	-	-	ns
Data setup time	$t_{DSW}$	195	-	-	ns
Data delay time	$t_{DDR}$			320	ns
Data hold time (write)	$t_H$	10	-		ns
Data hold time (read)	$t_{DHR}$	20	-	-	ns

Timing chart: See Fig. 1.

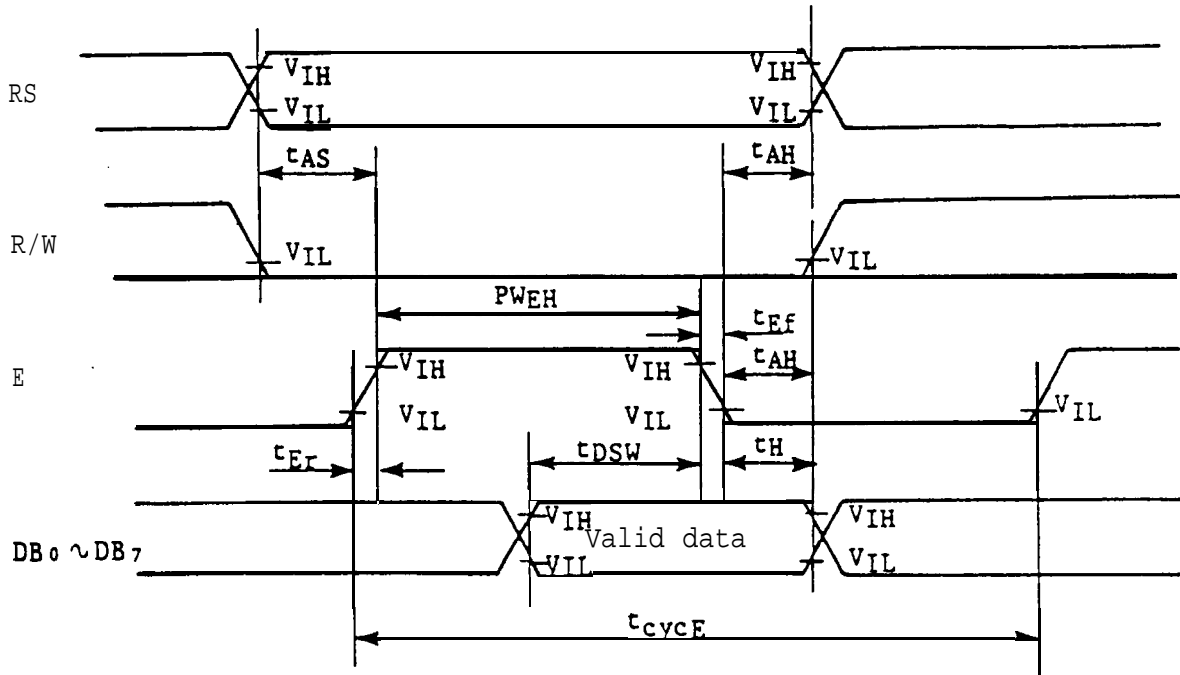
4.4 Interface signals

Table 5

Pin No.	Symbol	Description	Connection
1	$V_{SS}$	Ground potential	GND : 0V
2	$V_{DD}$	Power supply	+5V
3	$V_0$	Contrast adjustment voltage	Adjust the contrast by changing the supply voltage from 0V to 5V.
4	RS	Register select signal	Control signal inputs (For details, see section 6 and 7.)
5	R/W	Read/write select signal	
6	E	Operation(data read/write enable signal)	
7	$DB_0$	Code I/O data LSB	Data bus line · $DB_7$ may also be used to check the busy flag.  · Lines $DB_0 \sim DB_3$ are not used when interfacing with a 4-bit microprocessor. (For details, see section 6 and 7.)
8	$DB_1$	Code I/O data 2nd bit	
9	$DB_2$	Code I/O data 3rd bit	
10	$DB_3$	Code I/O data 4th bit	
11	$DB_4$	Code I/O data 5th bit	
12	$DB_5$	Code I/O data 6th bit	
13	$DB_6$	Code I/O data 7th bit	
14	$DB_7$	Code I/O data MSB	



Write Operation



Read Operation

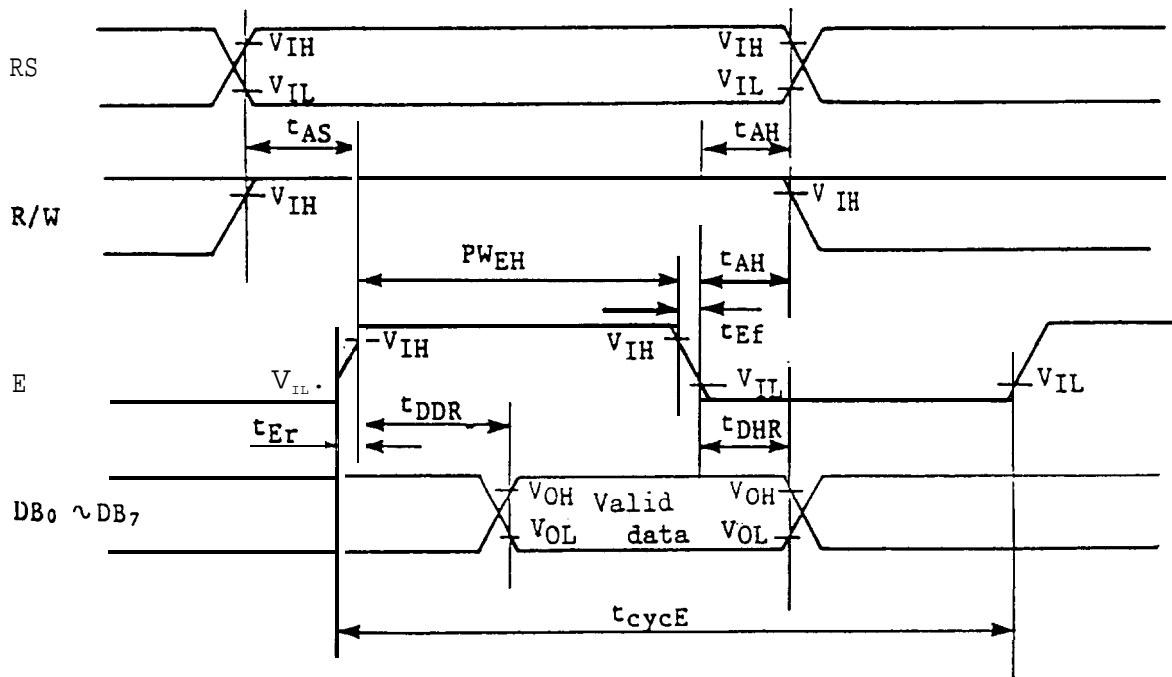


Fig. 1 Timing Chart

**SHARP**

## 5. Optical Characteristics

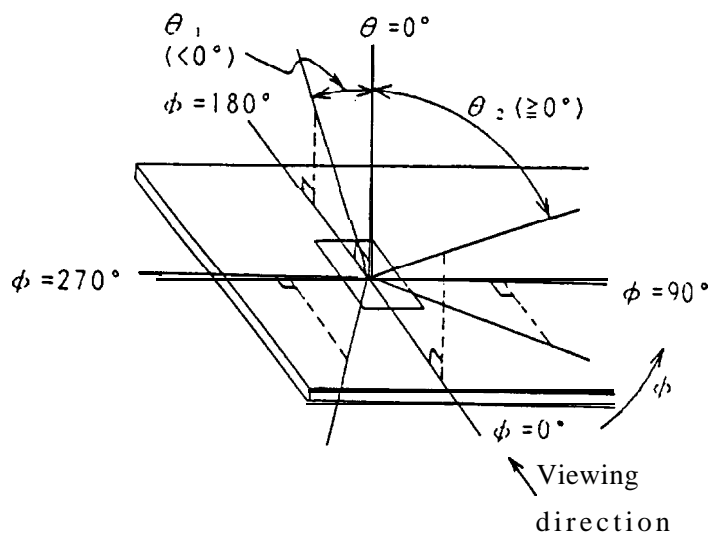
Table 6 shows the optical characteristics when LCD drive voltage is adjusted to the maximum contrast in  $\theta = 0^\circ$ .

Table 6

(Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	
Viewing angle range	$\theta_2 - \theta_1$	$\phi = 0^\circ$ $C_0 \geq 2.0$	60	-	-	dgr.	Note 1	
	$\theta_1$	$\theta_1 < \theta_2$ $C_0 = 2.0$	-	-	-25	dgr.	Note 1	
	$\theta_2$		25	-	-			
	Viewing angle range	$\theta_2 - \theta_1$	$\phi = 45^\circ$ $C_0 \geq 2.0$	60	-	-	dgr.	Note 1
		$\theta_1$	$315^\circ$ $C_0 = 2.0$	-	-	-25	dgr.	Note 1
		$\theta_2$		25	-	-		
Contrast ratio	$C_0$	$\theta = 0^\circ, \phi = 0^\circ$	3.0	5.0	-		Note 2	
Response time	Rise	$e = 0^\circ, \phi = 0^\circ$	-	150	250	ms	Note 3	
	Decay	$\theta = 0^\circ, \phi = 0^\circ$	-	150	250	ms	Note 3	

Note 1) The viewing angle range is defined as shown below.



\* Angles  $\theta_1, \theta_2$  and  $\phi$  shall fall within the range over which the displayed character can be read.

Fig.2 Definition of viewing angle

**SHARP**

Note 2) Contrast ratio is defined **as** follows:

When input signal is applied to the unit to select (turn on) the LCD dots (**pixels**) to be measured in the optical characteristics test method as defined in Fig. 3.

$$\text{Contrast ratio} = \frac{\text{Photodetector output voltage with non-select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$

Measurement wave length  $\lambda = 580\text{nm}$

Note 3) When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Fig. 3. The response characteristics of the photo-detector output are measured as shown in Fig. 4.



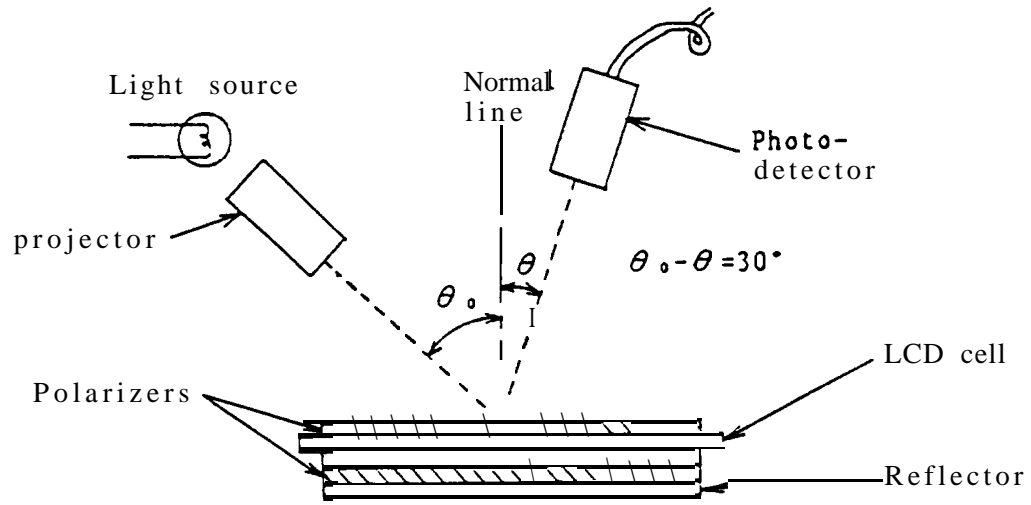


Fig. 3 Optical Characteristics Test Method

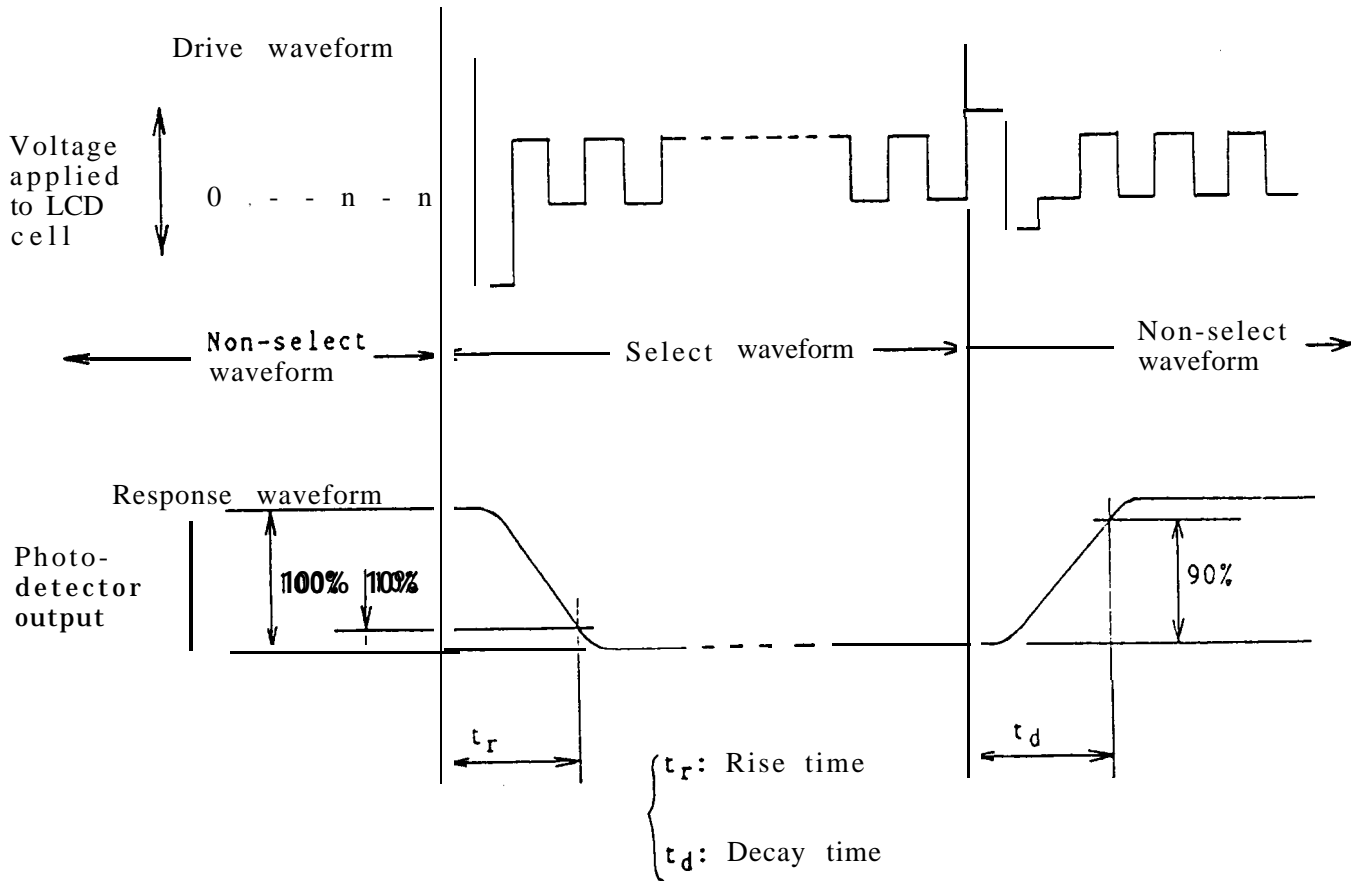


Fig. 4 Definition of Response Time

# SHARP

## 6. Pin Description

### 1) $V_{DD}$ and $V_{SS}$ Pins

$V_{DD}$  and  $V_{SS}$  pins are for power supply.  $V_{SS}$  pin is "grounded, and  $V_{DD}$  pin is supplied with +5V. Each voltage necessary to drive LCD is generated in the unit.

### 2) RS Pin

The controller LSI has two 8-bit registers; an instruction register (IR) and a data register (DR). RS signal selects these registers.

IR stores instruction codes such as display clear, shift, etc. and also stores address information for the display data RAM (DD RAM), character generator RAM (CG RAM); DR is used for temporarily storing data to be written into DD RAM and CGRAM.

" 0 " :Instruction register (when writing)

Busy flag register; address counter (when reading)

" 1 " :Data register (read/write)

### 3) R/W Pin

Read or write select signal pin.

" 0 " :Writing

" 1 " :Reading

### 4) E Pin

Data read or write operation enable signal pin.

### 5) $DB_0 \sim DB_7$ Pins

Data bus with three-state, bidirectional function for use in data transactions with MPU.  $DB_7$  may also be used to check the busy flag.

$DB_0 \sim DB_3$  are not used when interfacing with a 4 - bit microprocessor.

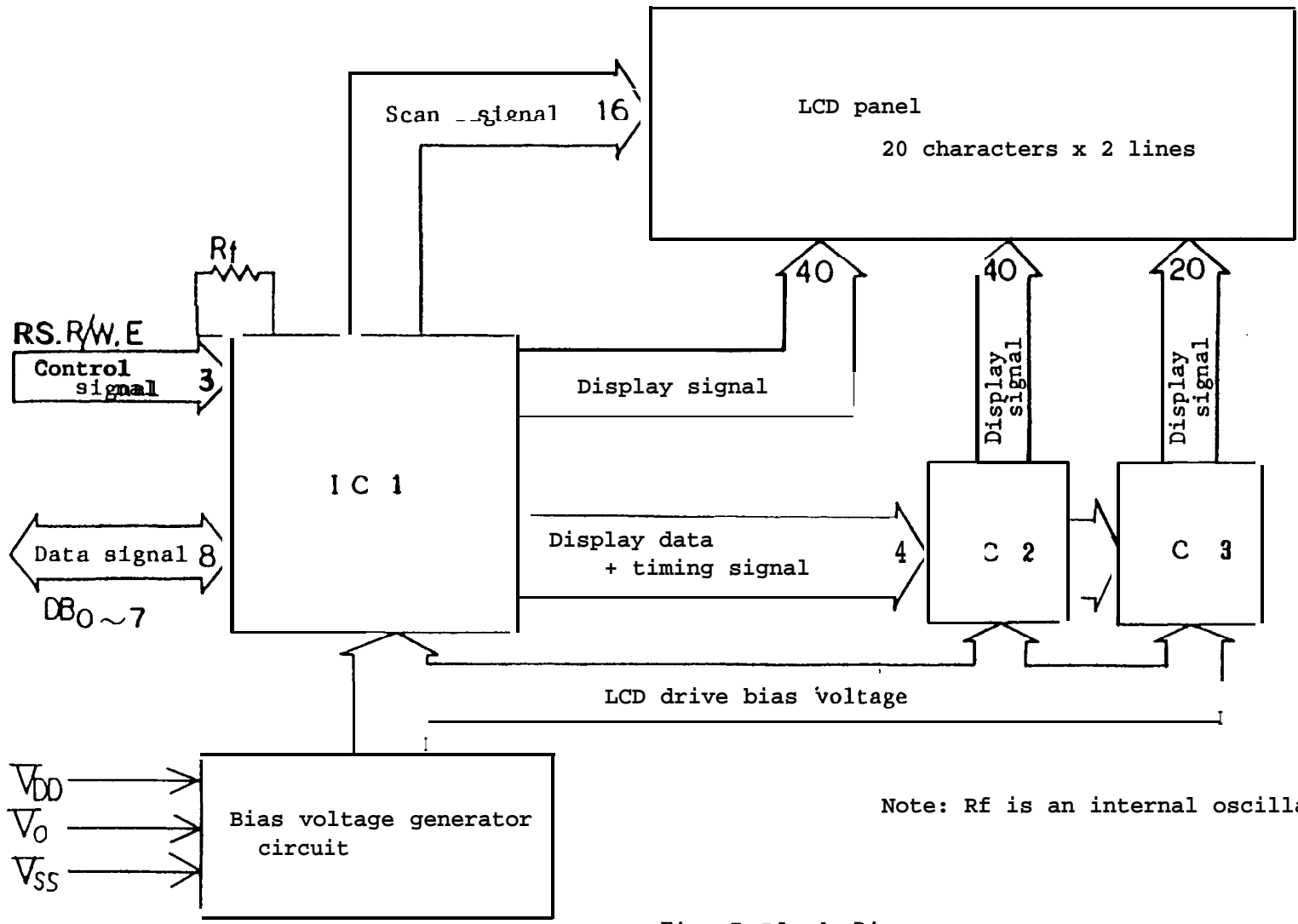
### 6) $V_0$ Pin

Viewing angle is varied and contrast is adjusted by changing voltage between +5V ~ 0V by applying bias voltage to the LCD driver.

7. Instruction Set

Table 7

Instruction	Code										Function																				
	RS	R/W	DB <sub>7</sub>	DB <sub>6</sub>	DB <sub>5</sub>	DB <sub>4</sub>	DB <sub>3</sub>	DB <sub>2</sub>	DB <sub>1</sub>	DB <sub>0</sub>																					
Display clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area, restore display from shift, and load address counter with DDRAM address 00H.																				
Display/cursor home	0	0	0	0	0	0	0	0	1	0	Restore display from shift and load address counter with DDRAM address 00H.																				
Entry mode set	0	0	0	0	0	0	0	1	I/D	s	Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.																				
Display ON/OFF	0	0	0	0	0	0	1	D	c	B	specify activation of display (D), cursor (C), and blinking of character at cursor position (B).																				
Display/cursor shift	0	0	0	0	0	1	S/C	R/L	0	*	Shift display or move cursor.																				
Function set	0	0	0	0	1	DL	1	0	*	0	Set interface data length (DL).																				
CGRAM address set	0	0	0	1	ACG						Load the address counter with a CC RAM address. Subsequent data is CC RAM data.																				
DD RAM address set	0	0	1	ADD						Load the address counter with a DD RAM address. Subsequent data is DD RAM data.																					
Busy flag/address counter read	0	1	BF	AC						Read busy flag (BF) and contents of address counter (AC).																					
CGRAM/DD RAM data write	1	0	Write data						Write data to CC RAM or DD RAM.																						
CC RAM/DD RAM data read	1	1	Read data						Read data from CGRAM or DD RAM.																						
<table border="0" style="width: 100%;"> <tr> <td style="width: 33%;">I/D-1: increment,</td> <td style="width: 33%;">I/D-0: Decrement</td> <td style="width: 33%;">S/C-1: Shift display,</td> <td style="width: 33%;">S/C-0: Move cursor</td> </tr> <tr> <td>S-1: Shift display,</td> <td>s-0: Freeze display</td> <td>R/L-1: Shift right,</td> <td>R/L-0: Shift left</td> </tr> <tr> <td>D-1: Display ON,</td> <td>D-0: Display OFF</td> <td>DL-1: 8-bit,</td> <td>DL-0: 4-bit</td> </tr> <tr> <td>c-1: Cursor ON,</td> <td>c-0: Cursor OFF</td> <td>BF-1: During internal operation,</td> <td>BF-0: End of internal operation</td> </tr> <tr> <td>B-1: Character at cursor position blinks,</td> <td>B-0: Character at cursor position unblinks</td> <td></td> <td></td> </tr> </table>												I/D-1: increment,	I/D-0: Decrement	S/C-1: Shift display,	S/C-0: Move cursor	S-1: Shift display,	s-0: Freeze display	R/L-1: Shift right,	R/L-0: Shift left	D-1: Display ON,	D-0: Display OFF	DL-1: 8-bit,	DL-0: 4-bit	c-1: Cursor ON,	c-0: Cursor OFF	BF-1: During internal operation,	BF-0: End of internal operation	B-1: Character at cursor position blinks,	B-0: Character at cursor position unblinks		
I/D-1: increment,	I/D-0: Decrement	S/C-1: Shift display,	S/C-0: Move cursor																												
S-1: Shift display,	s-0: Freeze display	R/L-1: Shift right,	R/L-0: Shift left																												
D-1: Display ON,	D-0: Display OFF	DL-1: 8-bit,	DL-0: 4-bit																												
c-1: Cursor ON,	c-0: Cursor OFF	BF-1: During internal operation,	BF-0: End of internal operation																												
B-1: Character at cursor position blinks,	B-0: Character at cursor position unblinks																														



Note: Rf is an internal oscillating resistor.

Fig. 5 Block Diagram

**SHARP**

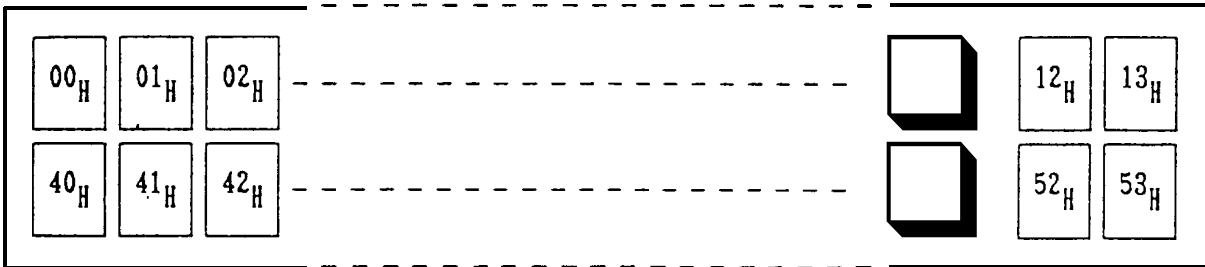


Fig.6 Display Address ( When the display is not shifted )

Table 8 Input Code vs. Character Pattern

*1 *2 4bit 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
XXXX0000	CG RAM (1)		Q	P	'	F			9	E	Q	*	
XXXX0001	(2)	U	H	A	A	A	A	A	A	A	A	A	*
XXXX0010	(3)	"	B	B	B	B	B	B	B	B	B	*	Q
XXXX0011	(4)	#	C	S	C	A	A	A	A	A	A	*	Q
XXXX0100	(5)	\$	D	T	A	T	A	A	A	A	A	*	Q
XXXX0101	(6)	%	E	V	E	A	A	A	A	A	A	*	Q
XXXX0110	(7)	&	F	V	V	V	V	V	V	V	V	*	Q
XXXX0111	(8)	'	G	W	W	W	W	W	W	W	W	*	Q
XXXX1000	(1)	(	H	X	X	X	X	X	X	X	X	*	Q
XXXX1001	(2)	)	Y	Y	Y	Y	Y	Y	Y	Y	Y	*	Q
XXXX1010	(3)	*	Z	Z	Z	Z	Z	Z	Z	Z	Z	*	Q
XXXX1011	(4)	+	K	K	K	K	K	K	K	K	K	*	Q
XXXX1100	(5)	,	L	L	L	L	L	L	L	L	L	*	Q
XXXX1101	(6)	-	M	M	M	M	M	M	M	M	M	*	Q
XXXX1110	(7)	.	N	N	N	N	N	N	N	N	N	*	Q
XXXX1111	(8)	/	O	O	O	O	O	O	O	O	O	*	Q

Note 1. CG RAM is character generator RAM in which user-definable character pattern are stored.

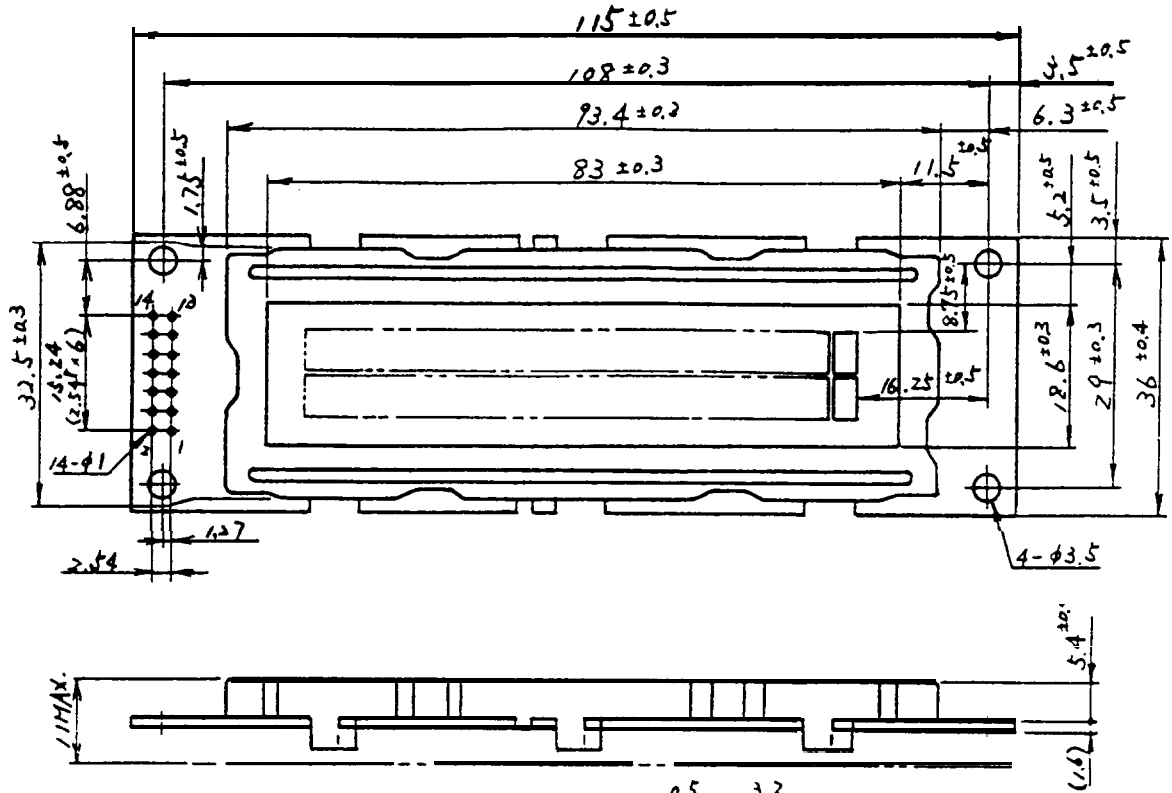
Note 2. Xmark: prohibition of input

\*1 High-order \*2 Low-order

**SHARP**

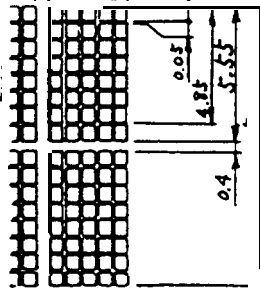
<b>出図</b>	19 . . .
ISSUE	
<b>設計通報</b>	<b>連絡書</b>
DRAWING INFO.	INFORMATION
No. ( ) 号によ	
<b>新設・変更・書換</b>	<b>図面</b>
NEW CHANGE REPLACE.	

Fig.7 Unit Outline Dimensions and Pin Connections



N No.	Sig.	PIN No.	Sig.
4	DB7	13	DB6
2	DB5	11	DB4
0	DB3	9	DB2
3	DB1	7	DB0
5	E	5	R/W
1	RS	3	V <sub>0</sub>
2	V <sub>DD</sub>	1	V <sub>SS</sub>

Character Pattern Details



指示なき寸法公差は とする  
UNSPECIFIED TOL TO BE

19 . . .						名称	Outline Dimensions and Pin Connections
19 . . .					LM20A21	NAME	
年月日	訂正記事	投通No.	担当	適用機種		記号	
DATE	RMSE	PREPA	MODEL			SYMBOL	
材	質	板厚	仕	上	尺度	部品コード	
MATERIAL	THICKNESS	FINISH			1/1	PARTS CODE	
設計	写図	検図	検図	承認		作成日付	1988. 6. 16.
TRACE	CHECK	CHECK	APPROVE			DATE	
					<b>シャープ株式会社</b>	図番	OD20A21-301C
					<b>SHARP CORPORATION</b>	DRAWING No.	
					発行部門		
					LCD Division		